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SPECIFICATION

MOS TRANSISTOR HAVING IMPROVED TOTAL RADIATION-INDUCED LEAKAGE CURRENT AND METHOD FOR FABRICATING SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to MOS transistors. More particularly, the present invention relates to MOS transistors having improved total radiation-induced leakage currents.

2. The Prior Art

It is known that MOS transistors exhibit increased radiation-induced leakage along channel ends at the birds beak region of the field oxide edges caused by electron-hole pair charge buildup. This effect is only seen in n-channel devices. P-channel devices are not negatively affected. It is known to reduce this radiation-induced current leakage by increasing the boron field channel-stop

implant dose under the birds beak edges of the field oxide isolation regions. Typically, field channel-stop implant doses may be increased from about 6e13 up to about 1.2e14.

While increasing the field channel-stop implant dose is known to decrease this radiation-induced current leakage, the increased field channel-stop implant dose has the unwanted effect of decreasing the junction breakdown voltage of the MOS transistor. The need to avoid unwanted lowering of the junction breakdown of the transistor limits the use of increased field channel-stop implant dose as a means of decreasing the radiation-induced current leakage in MOS transistors.

Recently, shallow-trench isolation has been used as an isolation technique. Use of this technique, in which trenches are etched in the silicon substrate and filled with deposited silicon dioxide, provides a deep isolation and a much more planarized surface than can be obtained by using the traditional field oxide isolation techniques. In transistors formed using shallow-trench isolation techniques, the top surface of the silicon dioxide at the edges of the trenches can

lie below the level of the bottom of the source/drain implants in the active transistor regions. The polysilicon gates formed over the gate oxides of the transistors follow the contours formed by the lowered edges of the silicon dioxide used to fill the trenches and thus can also extend vertically below the level of the bottom of the source/drain implants in the active transistor regions. Because there is no field channel-stop implant in the shallow-trench isolation structures, radiation-induced current leakage can occur at the edges of the source and drain regions where the polysilicon transistor gate extends below the source and drain implants.

Attempts have been made to correct this problem by modifying the geometries of the silicon and silicon dioxide interface at the trench edges. These attempts have met with varying degrees of success.

BRIEF DESCRIPTION OF THE INVENTION

A shallow-trench isolation transistor according to the present invention includes a sidewall channel-stop implant around the side and bottom walls of the trench. This implant extends below the level of the source and drain implants in

the active transistor region and significantly lowers the radiation-induced leakage currents that would otherwise exist in the shallow-trench isolation transistor.

A method for fabricating a shallow-trench isolation transistor according to the present invention includes forming isolation trenches to define active regions in a silicon substrate; performing sidewall isolation impants on the side and bottom walls of the isolation trenches in the n-channel (p-well) areas only; depositing a dielectric isolation material in the isolation trenches; planarizing the top surface of the silicon substrate and the dielectric isolation material using CMP techniques; forming a gate oxide layer over the active regions in the silicon substrate; forming and defining gate regions over the gate oxide layer in the active regions in the silicon substrate; and forming source and drain regions in the active regions in the silicon substrate. The method of the present invention requires the use of one additional mask for sidewall implant in the n-channel (p-well) areas only.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

FIG. 1 is a cross-sectional view of a conventional field oxide isolated MOS transistor.

FIG. 2 is a cross-sectional view of a conventional shallow-trench isolated MOS transistor.

FIG. 3 is a cross-sectional view of a shallow-trench isolated MOS transistor according to the present invention

FIGS. 4A through 4C are cross-sectional views of a shallow-trench isolated MOS transistor showing the structure formed at different times during the progression of a fabrication process according to the method of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other

embodiments of the invention will readily suggest themselves to such skilled persons.

Referring first to FIG. 1, a cross-sectional view taken at the channel end of a conventional field oxide isolated MOS transistor 10 is shown. Transistor 10 is formed in silicon substrate 12 between two field oxide isolation regions 14 as is well known in the art. Gate oxide layer 16 insulates polysilicon gate 18 from the surface of substrate 12. Channel stop field implants 20, usually comprising a boron implant, underlie the birds beak edges of the field oxide regions.

The structure of FIG. 1 is well known in the art. It is known that MOS transistors such as the one illustrated in FIG. 1 exhibit increased radiation-induced leakage along channel ends at the birds beaks at the edges of the field oxide regions 14 caused by electron-hole pair charge buildup. It is known to reduce this radiation-induced current leakage by increasing the dose of the field channel-stop implant 14 under the birds beak edges of the field oxide isolation regions 14. Typically, field channel-stop implant doses may be increased from about 6e13 atoms/cm^2 up to about 1.2e14 atoms/cm^2.

As previously noted, while increasing the field channel-stop implant dose is known to decrease this radiation-induced current leakage, the increased field channel-stop implant dose has the unwanted effect of decreasing the junction breakdown voltage of the MOS transistor 10. The need to avoid unwanted lowering of the junction breakdown of the MOS transistor 10 limits the use of increased field channel-stop implant dose as a means of decreasing the radiation-induced current leakage in MOS transistors.

Referring now to FIG. 2, a cross-sectional view taken at the channel end of a conventional shallow-trench isolated MOS transistor 30 is shown. Transistor 30 is formed in silicon substrate 32 between two shallow trench isolation structures filled with deposited silicon dioxide 34 as is well known in the art. Gate oxide layer 36 insulates polysilicon gate 38 from the surface of substrate 32. Unlike transistor 10 of FIG. 1, no channel-stop field implants are employed.

In transistors 32 formed using shallow-trench isolation techniques, edges 40 of the top surface of the silicon dioxide regions 34 at the edges of the trenches can

lie below the level of the bottom of the source/drain implants (not shown) in the active transistor regions 42. The polysilicon gates 38 formed over the gate oxides 36 of the transistors 32 follow the contours formed by the lowered top surfaces 40 of the silicon dioxide regions 34 used to fill the trenches and thus can also extend vertically below the level of the bottom of the source/drain implants in the active transistor regions 42. Because there is no field channel-stop implant in the gate edge region of conventional shallow-trench isolation structures, radiation-induced current leakage can occur at the edges of the source and drain regions where the polysilicon gate 38 of MOS transistor 32 extends below the source and drain implants.

Referring now to FIG. 3, a cross-sectional view of a shallow-trench isolated MOS transistor 50 illustrates the features of the present invention. Shallow-trench isolated MOS transistor 50 is formed in silicon substrate 52 between two shallow trench isolation structures filled with deposited silicon dioxide 54 as in the prior-art shallow-trench isolated MOS transistor of FIG. 2. Gate oxide layer 56 insulates polysilicon gate 58 from the surface of substrate 52.

Unlike the prior-art shallow-trench isolated MOS transistor of FIG. 2, a sidewall implant 60 is formed in the walls of the isolation trenches prior to the deposition of the oxide fill regions 54. The implant is performed at an angle so that it penetrates the sidewalls of the trenches. The substrate may be rotated or other techniques may be employed to assure implanting all four of the sidewalls.

As will be appreciated by persons of ordinary skill in the art, different species will be used for the sidewall implant 60 depending on whether N-Channel or P-Channel MOS transistors are being formed. For example, to form N-Channel MOS transistors according to the present invention, boron may be implanted at a dose of about 2.0e12. P-Channel MOS transistors do not need the sidewall trench implant according to the present invention.

Turning now to FIGS. 4A through 4C, a method for fabricating shallow-trench isolated MOS transistors according to the present invention is illustrated. FIGS. 4A through 4C are cross-sectional views of a shallow-trench isolated MOS transistor showing the structure formed at different times during the progression of a fabrication process according to the method of the present invention. Structures

in FIGS. 4A through 4C corresponding to structures in FIG. 3 will be given the same reference numerals as seen in FIG. 3.

Referring now to FIG. 4A, substrate 52 is shown after formation of isolation trenches 62. As will be appreciated by persons of ordinary skill in the art, isolation trenches 62 are formed using conventional masking and etching techniques to a depth of about 400nm, after which the mask layer is removed using conventional semiconductor processing techniques.

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As shown in FIG. 4A, sidewall implants 60 are formed in the side and bottom walls of isolation trenches 62. As will be appreciated by persons of ordinary skill in the art, sidewall implants 60 may be formed using an angled ion-implant process during which the substrate 52 may be rotated as known in the art to assure coverage of all of the sidewalls of the isolation trenches 62. FIG. 4A shows the structure existing after the performance of the sidewall implant step for one type of transistor before removal of implant mask layer 64.

In accordance with the present invention, sidewall implants for isolation of N-Channel MOS transistors according to the present invention may be performed by, for example, implanting boron at a concentration of about 2.0e12 at an angle of about 25°.

Referring now to FIG. 4B, implant mask layer 64 has been removed. Silicon dioxide regions 54 have been formed in trenches 62 using conventional CVD or PECVD techniques and the surfaces of silicon dioxide regions 54 and the top surface of substrate 52 have been planarized using conventional CMP techniques. Note that, as an artifact of the planarizing process and oxide etching steps, the edges of the top surface of silicon dioxide regions 54 lie below the edges of isolation trenches 62.

Referring now to FIG. 4C, gate oxide layer 56 and polysilicon gate layer 58 have been formed and defined using conventional photolithographic and semiconductor processing techniques. Source and drain regions (outside of the plane of the cross-section of FIG. 4C and therefore shown as dashed lines 66) are implanted using the edges of the gate 58 as a mask in a conventional self-aligned

gate process sequence. Note that the polysilicon gate regions adjacent to the edges of the isolation tenches 62 lie below the level of the source and drain implants.

Persons of ordinary skill in the art will understand that, after performing the steps illustrated in FIGS. 4A through 4C, other conventional and well known processing steps, such as passivation and contact formation (not shown), will need to be performed top complete the integrated circuit.

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.